IN THE CLAIMS

Please amend the claims to the following:

1. (Currently Amended) A method comprising:

receiving from a processor a plurality of write transactions ~~to be~~ write combined ~~from~~ in a processor;

storing data associated with the plurality of write transactions ~~to~~ in a buffer of an input/output (I/O) hub to form write combined data; and

flushing the write combined data associated with the plurality of write transactions to an I/O device according to a protocol between the I/O hub and the processor.

2. (Original) The method of claim 1, wherein flushing the data to the I/O device includes:

determining whether a flush signal has been received from the processor; and

flushing the data if the flush signal has been received, the protocol including an signaling protocol.

3. (Original) The method of claim 2, further including sending a write completion signal to the processor for each of the write transactions before the data is flushed to the I/O device, each write completion signal verifying buffering of a corresponding write transaction.

4. (Original) The method of claim 3, further including sending a flush completion signal to the processor after the data is flushed to the I/O device.

5. (Original) The method of claim 2, wherein flushing the data if the flush signal has been received further includes:

tagging the buffer with a first source identifier associated with one or more of the write transactions;

detecting a second source identifier associated with the flushing signal;

comparing the second source identifier to the first source identifier; and

flushing the data to the I/O device if the second source identifier matches the first source identifier.

6. (Original) The method of claim 5, further including repeating the comparing for a plurality of buffers, each buffer corresponding to an I/O port.

7. (Original) The method of claim 1, wherein flushing the data to the I/O device includes:

determining whether a latency condition exists; and

flushing the data if the latency condition exists, the protocol including a timing protocol.

8. (Original) The method of claim 7, further including sending a write completion signal to the processor for each of the write transactions as the data is flushed to the I/O device, each write completion signal verifying flushing of a corresponding write transaction.

9. (Original) The method of claim 7, wherein the latency condition includes a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state.

10. (Original) The method of claim 1, wherein flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device.

11. (Original) The method of claim 1, wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining, each of the plurality of write transactions including one of the plurality of commands.

12. (Currently Amended) An input/output (I/O) hub comprising:

~~a buffer; and~~

~~a write combining module to:~~

receiving logic to receive a ~~plurality of~~ first and a second write transaction, the first and the second write transactions write combined in ~~transactions determined to be write combined from~~ a processor,

storage logic coupled to the receiving logic to store data associated with the ~~plurality of~~ first and second write transactions as write combined data ~~to the buffer~~ and

flushing logic coupled to the storage logic to flush the write combined data to an I/O device in response to a protocol event ~~according to a protocol between the I/O hub and the processor~~.

13. (Currently Amended) The I/O hub of claim 12, wherein the protocol event includes special flush signal to be received by the receiving logic from the processor. ~~the write combining module is to determine whether a flush signal has been received from the processor and flush the data if the flush signal has been received, the protocol to include an signaling protocol.~~

14. (Currently Amended) The I/O hub of claim 13, ~~wherein the write combining module is~~ further comprising transmission logic to send a first and a second write completion signal to the processor for ~~each of~~ the first and the second write transactions, respectively, before the write combined data is flushed to the I/O device, wherein ~~each~~ the first and the second write completion ~~signal~~ signals are to verify successful storage of data associated with the first and the second ~~buffering of a corresponding~~ write ~~transaction~~ transactions, respectively.

15. (Currently Amended) The I/O hub of claim 14, wherein ~~the write combining module~~ the transmission logic is also to send a flush completion signal to the processor after the write combined data is flushed to the I/O device.

16. (Currently Amended) The I/O hub of claim 12, further comprising ~~wherein the~~ write combining logic ~~module is~~ to determine whether a latency condition exists, wherein the protocol event includes the latency condition ~~and flush the data if the latency condition exists, the protocol to include a timing protocol.~~

17. (Currently Amended) The I/O hub of claim 16, further comprising ~~wherein the~~ transmission logic ~~combining module is~~ to send a first and a second write completion signal to the processor for ~~each of~~ the first and the second write transactions, respectively, as the write combined data is flushed to the I/O device, wherein ~~each~~ the first and the second write completion ~~signal~~ signals are to verify flushing of ~~a corresponding~~ the first and the second write ~~transaction~~ transactions, respectively.

18. (Currently Amended) The I/O hub of claim 16, wherein the latency condition includes a delay in receiving a next third combinable write transaction from the processor and an interface to the I/O device being in an idle state.

19. (Currently Amended) The I/O hub of claim 12, ~~further~~ wherein the storage logic includes ~~including~~ a plurality of buffers, each buffer corresponding to an I/O port, and wherein the flushing logic ~~the write combining module~~ is to ~~store data to and~~ flush data from the plurality of buffers in response to a protocol event ~~according to the protocol between the I/O hub and the processor~~.

20. (Currently Amended) The I/O hub of claim 12, wherein the write combined data is to be longer than one cache line.

21. (Currently Amended) A system comprising:

an input/output (I/O) device;

a peripheral components interconnect (PCI) express bus coupled to the I/O device;

a processor; and

a chipset having an I/O hub coupled to the PCI express bus and the processor, the I/O hub having a buffer and a write combining module to receive a plurality of write transactions to be write combined from the processor, to store data associated with the plurality of write transactions ~~to~~ in the buffer to form a write combined data set and to flush the write combined data set to the I/O device ~~according to~~ in response to a protocol event associated with the processor ~~between the chipset and the processor~~, the data to be longer than one cache line.

22. (Currently Amended) The system of claim 21, wherein the protocol event includes a flush signal from the processor ~~the write combining module is to determine whether a flush signal has been received from the processor and flush the data if the flush signal has been received, the protocol to include a signaling protocol~~.

23. (Currently Amended) The system of claim 22, wherein the processor is to generate the ~~flushing~~ flush signal if a flushing event has occurred and a write combine history indicates that one or more combinable write transactions have been issued by the processor.

24. (Original) The system of claim 23, wherein the write combine history is to track combinable write transactions for a particular processor thread.

25. (Original) The system of claim 24, wherein the write combine history is to further track combinable write transactions for a particular I/O hub.

26. (Currently Amended) The system of claim 22, wherein the chipset includes a plurality of I/O hubs, the processor to send the ~~flushing~~ flush signal to each of the plurality of I/O hubs.

27. (Currently Amended) The system of claim 26, wherein the processor is to verify that one or more combinable write transactions have been sent to each of the plurality of I/O hubs before sending the ~~flushing~~ flush signal.

28. (Currently Amended) The system of claim 21, wherein the protocol event includes a latency condition ~~the write combining module is to determine whether a latency condition exists and flush the data if the latency condition exists, the protocol to include a timing protocol~~.

29. (Original) The system of claim 21, wherein the processor is to instruct the I/O hub to consider each write transaction for write combining based on a page table attribute associated with the write transactions.

30. (Original) The system of claim 21, further including a point-to-point network interconnect coupled to the processor and the I/O hub, the network interconnect having a layered communication protocol.

31. (Original) A method comprising:

receiving a plurality of write transactions from a processor, the plurality of write transactions being destined for an input/output (I/O) device;

storing data associated with the plurality of write transactions to a buffer of the I/O hub;

determining whether a latency condition exists, the latency condition including a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state;

flushing the data to the I/O device if the latency condition exists; and

sending a write completion signal to the processor for each of the plurality of write transactions as the data is flushed to the I/O device, each write completion signal verifying flushing of a corresponding write transaction.

32. (Original) The method of claim 31, wherein flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device.

33. (Original) The method of claim 31, wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining, each of the plurality of write transactions including one of the plurality of commands.

34. (Currently Amended) A machine readable medium to store a set of instructions that direct a computer to function in a specified manner when executed, the instructions comprising:

receiving a plurality of write transactions to be write combined from a processor;

storing data associated with the plurality of write transactions ~~to~~ in a buffer of an input/output (I/O) hub to form a write combined data set; and

flushing the write combined data set to an I/O device in response to a protocol event according to a protocol between the I/O hub and the processor.

35. (Original) The medium of claim 34, wherein the protocol event includes a flushing signal from the processor, and wherein ~~flushing the data to the I/O device is to include: determining whether a flush signal has been received from the processor; and flushing the data if the flush signal has been received,~~ the protocol is to include an signaling protocol.

36. (Original) The medium of claim 34, wherein the protocol event includes a latency condition, and wherein ~~flushing the data to the I/O device is to include:~~

~~determining whether a latency condition exists; and~~

~~flushing the data if the latency condition exists,~~ the protocol to include a timing protocol.